[the]
of said packaging substrate, and the packaging substrate is a mounting substrate for forming a specified circuit by mounting the semiconductor package thereon.

REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority, and for confirming that a copy of the Priority Document has been received by the Patent Office. Applicant also thanks the Official Draftsperson for accepting the drawings filed on **June 7, 2001**. As a final matter, Applicant thanks the Examiner for considering the reference submitted with the Information Disclosure Statement dated **July 17, 2001**, as evidenced by the initialed PTO-1449 Form.

The Examiner has objected to the specification under 35 USC § 112, first paragraph, as being unclear. Further, claim 3 stands rejected under 35 USC § 112, second paragraph, as being indefinite. Applicant has amended the specification and claim 3 as shown herein to address the §112 rejections.

Claims 1-11 stand reject under the 35 USC § 103(a) as being unpatentable over U.S. Patent Application Publication, App. No. 09/203196 (Yoon *et, al.*), in view of Lyne (U.S. Patent No. 6,285,560) and Katz (U.S. Patent No. 6,310,398). Because there is no motivation to combine these references, Applicant respectfully traverses the prior art rejection based on the following remarks.

Yoon discloses that lead frame 11 has eight conductors 10a as shown in Fig. 3A such that the number of lead frames can be reduced to one-eighth, On the other hand, Lyne discloses selectively depopulating soldered balls from a solder grid array (BGA) depending on a trace between standard vias, and traces between depopulated vias. Moreover, Katz discloses groups of terminals organized into a plurality of radial spokes extending from the center to the outer perimeter and disposing traces between each of the radial spokes.

According to the present invention, the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The I/O is a single group including a single unit having one or more input-output buffers formed in the chip 13 and an S-terminal (single line terminal), V-terminal (power source terminal) and G-terminal (ground terminal) connected to the input-out-put buffers, or the single I/O cell may include only S-terminals. (Specification pg. 12, line 19- pg. 13, line 4).

In the present invention, a designing method is disclosed for grouping interconnect lines as a single I/O cell (or a block) having a combination of signal/ground/power without dividing the group. The interconnect lines are designed as the same length for the I/O cell and do not cross one another such that connection delays between the lines are reduced and impedance is matched. The density of the interconnect lines is increased by optimizing a space between the I/O cells while maintaining the quality of the signals.

The Examiner admits that Yoon does not explicitly disclose a mounting member including a plurality of electrode terminals electrically and mechanically connected

to respective interconnect pads for mounting a semiconductor chip on a mounting member. Instead, Applicant respectfully submits that the Examiner incorrectly asserts that it would be obvious to modify Yoon's packaging substrate to provide for a mounting member to obtain the advantage of having electrical and mechanical functioning connections to provide for a functioning electrical device.

As shown in Fig. 4 of Yoon, Yoon's package body 20 includes four layers. [0046] Each of Yoon's package layers is heat-adhered to each other by pressure and the via holes are filled with conductive paste T. [0047]. Accordingly, it is clear that Yoon does not disclose, teach or suggest a semiconductor member and a mounting member as recited in independent claim 1.

The semiconductor member of claim 1 includes a plurality of interconnect pads 41. The mounting member (substrate 12) of claim 1 employs a plurality of electrode terminals (internal electrodes 31) which are electrically and mechanically connected to the interconnect pads of the semiconductor member (mounting substrate 14) for mounting the semiconductor chip 13. Of course, Yoon does not disclose, teach or suggest either a semiconductor member or a mounting member, or their recited connections.

In fact, because Yoon's package layers adhere to each other, it would impossible for Yoon, in and of itself, to disclose, teach or suggest the mounting member as recited in independent claim 1. The Examiner does not refer to either Lyne or Katz for the missing mounting member. Accordingly, there is no suggestion or motivation in any of the

applied prior art references to combine theses references (either alone or in combination) in order to meet the claimed limitations of the present invention.

Moreover, even if the applied references were combined, the resulting combination would not produce the claimed limitations of the present invention. Therefore, there would be no reasonable chance of success in obtaining the claimed features of the present invention upon the combination of the applied references. Accordingly, since the Examiner has not met the initial burden of proving a *prima facie* case, the rejection of claims 1-11 under 35 USC § 103 is improper.

Further, since claims 2-11 depend from independent claim 1, these claims are also patentable over the cited references for the same reasons as set out above with respect to independent claim 1. Accordingly, the § 103(a) rejection of claims 1-11 is improper.

Thus, for all the foregoing reasons, all the presently pending claims are believed to be allowable. Since all the presently pending claims are believed to be allowable, and since this application is believed to be otherwise in condition for allowance, Applicant respectfully requests that this application be passed to issue at the earliest possible time.

Respectfully submitted,

Eric Halber

Eric P. Halber
Registration No: 46,378

SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza
Garden City, New York 11530
516-742-4343
EPH:ko

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATIONS

Please amend pgs. 11, 12, 14, 16, and 17 as follows:

Pg. 11

The chip 13 is formed by a semiconductor substrate such as silicon, and various elements such as a transistor not shown in the drawing are formed on the bottom main surface of the chip 13 and are covered with a protective dielectric film such as a passivation film. On the surface of the protective dielectric film or on the bottom surface of the chip are formed and arranged ball electrodes 31 made of solder, connected to the above elements, acting as internal electrodes. The ball electrodes 31 are soldered to the interconnect pads 21 formed on the packaging substrate 12 to mount the chip 13 on the packaging substrate 12 in a face-down manner, and the elements in the chip 13 are electrically connected to the ball electrodes 24 on the bottom surface of the packaging substrate 12 through intermediary of the ball electrodes 31 and the interconnect pads 21. The chip 13 is sealed is sealing resin 28.

In the first embodiment, the semiconductor device 11 is mounted on a dielectric substrate, mounting substrate 14. A specified interconnect pattern is formed on the [a] dielectric substrate by using a conductive film to prepare the mounting substrate 14. The interconnect pattern includes interconnect[s] pads 41 connected to the ball electrodes 24 of the semiconductor device 11 and interconnect lines, not shown in the drawings, for connecting the

interconnect pads 41 among one another on the mounting substrate 14 or the interconnect pad 41 with interconnect lines not shown in the drawings for connecting the interconnect pad 41 to an external circuit.

An example of configuration will be described, referring to Fig. 4 [5], in which the ball electrodes 31 are formed and arranged on the bottom surface of the chip 13 of the semiconductor device 11 and interconnect pads 21 are formed and arranged on the top surface of the packaging substrate 12 corresponding to the ball electrodes 31.

The interconnect pads 21 formed on the top surface of the packaging substrate 12 shown in Fig.5 are disposed corresponding to the ball electrodes 31 on the bottom surface of the chip 13. The ball electrodes 31 on the bottom surface of the chip 13 are arranged in the shape of a lattice and the interconnect pads 21 are also arranged in the shape of the lattice corresponding to the ball electrodes 31. The specified number of the ball electrodes 31 and the interconnect pads 21 are grouped as a single I/O cell as shown in Fig.5 in which only the interconnect pads 21 are shown, and these are arranged as the I/O cell unit. In the embodiment, the plenty of the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The

22a are connected to each of the interconnect pads 21a of the two outer peripheral I/O cells (CELL-A), and are drawn between the interconnect pads 21a to regions external to the chip 13. On the other hand, the interconnect lines 22b are connected to each of the interconnect pads 21b of the inner peripheral I/O cell (CELL-B), and are drawn similarly to the preceding example in the region of the peripheral I/O cell (CELL-B), and are bundled at a specified interval, at a region out of the inner peripheral I/O cell (CELL-B), to be drawn between the outer peripheral I/O cells (CELL-A) to regions external to the chip 13.

In the structure of the interconnect pads 21 and the interconnect lines 22 on the packaging substrate 12, the density of arranging the interconnect lines 21a at the I/O cells (CELL-A) arranged on the outer periphery of the chip 13 is substantially same as the density of the conventional device shown in Fig.3. However, the density of arranging the interconnect lines 22b [21b] connected to the interconnect pad 21b of the I/O cells (CELL-B) arranged inside of the chip 13 can be increased because of the absence of the interconnect pads.

Especially, as shown in Fig.6, since the interconnect lines of the other I/O cells do not pass through the I/O cells (CELL-B) disposed on the inner section of the chip, the I/O cells (CELL-B) may be formed [endlessly or annually] to enable the arrangement of the extremely larger number of the ball electrodes 31 and the interconnect pads 21. An interval may exist between the I/O cells (CELL-B) disposed on the inner section. The ball electrodes 31 and the interconnect pads 21 of the outer peripheral I/O cells (CELL-A) may be freely disposed so long as the spaces through which the interconnect lines 22 of the I/O cells (CELL-B) disposed on the inner section pass may be secured, thereby promoting the higher integration of the semiconductor device having the higher performances. The I/O cells can be freely disposed in the regions of the chip so long as the above requisites are satisfied to increase the freedom of the chip design and the package design.

Since the interconnect pads 21 and the interconnect lines 22 in the embodiment are made by the conductive film having the single layer, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines.

Pg. 17

A second embodiment of the present invention is shown in Fig.7 in which the same numerals as those of the first embodiment designate the same elements. A semiconductor device 11 includes a packaging substrate 12A and a chip 13 mounted thereon. The packaging substrate 12A includes a central core layer 211 sandwiched between a pair of buildup layers 212, 213, and a plenty of interconnect pads 21 made of a conductive film are formed on the top buildup layer 212. The interconnect pads 21 are connected to the interconnect lines in each of the multi-layers of the top buildup layer 212, further connected to the bottom buildup layer 213 through intermediary of via plugs, and still further connected to ball electrodes 24 formed on the bottom surface of the bottom buildup layer 213 or the bottom surface of the packaging substrate 12A.

Each of the buildup layers is multi-layered, and the top buildup layer 212 includes five interconnect layers in which a first layer includes the interconnect pads 21 and a ground (GND) layer, a third layer includes a GND layer 3G and a voltage (VDD) layer 3V, and a fifth layer includes a GND layer 5G and a VDD layer 5V connected to the via plugs of the above core layer.

IN THE CLAIMS:

Please amend claim 3 as follows, without prejudice:

3. (Once amended) The semiconductor device as defined in claim 1, wherein the mounting member is a semiconductor package for mounting, a semiconductor chip on a packaging substrate, the electrode terminals are ball electrodes disposed on a bottom surface of [the] said packaging substrate, and the packaging substrate is a mounting substrate for forming a specified circuit by mounting the semiconductor package thereon.